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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/777,156	02/13/2004	Shuji Mayama	118678	4035
25944	7590	08/10/2005		
OLIFF & BERRIDGE, PLC			EXAMINER	
P.O. BOX 19928				KITOV, ZEEV
ALEXANDRIA, VA 22320			ART UNIT	PAPER NUMBER
			2836	

DATE MAILED: 08/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No.	Applicant(s)	
	10/777,156	MAYAMA ET AL.	
	Examiner	Art Unit	
	Zeev Kitov	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 11 July 2005.
- 2a) This action is **FINAL**. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1 - 12 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) 4 - 6 is/are allowed.
- 6) Claim(s) 1, 7 - 9 is/are rejected.
- 7) Claim(s) 2,3,10 and 12 is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 12 July 2004 is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

<ol style="list-style-type: none"> 1)<input checked="" type="checkbox"/> Notice of References Cited (PTO-892) 2)<input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) 3)<input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____. 	<ol style="list-style-type: none"> 4)<input type="checkbox"/> Interview Summary (PTO-413) Paper No(s)/Mail Date. _____. 5)<input type="checkbox"/> Notice of Informal Patent Application (PTO-152) 6)<input type="checkbox"/> Other: _____.
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DETAILED ACTION

Examiner acknowledges a submission of the amendment and arguments filed on July 11, 2005 after Final Office Action. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn. The Amendment is to be entered.

Claims 1, 2, 4, 5, 9, and 10 - 12 are amended. Amendment and arguments have overcome rejections under 102 (b) and 103(a).

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Izawa et al. (US 6,005,761) in view of Lee (US 5,764,035). Regarding Claims 1 and 4, Izawa et al. disclose an FET as an N-channel MOS transistor (element 18 in Fig. 2) provided upstream of the load with respect to a flow of power current, the FET controlling an activation state of the load, the protection circuit including: a first connection changer (element 20 in Fig. 2) interposed on a connection line between a

gate of the FET and a gate drive voltage supply source (elements 15 and 16 in Fig. 2), the first connection changer changing a connection state between a first connection state in which the gate is connected to the gate drive voltage supply and a second connection state in which the gate is connected to a ground (col. 14, line 65 24 – col. 15, line 13); the first connection line connects a gate of the FET and a gate drive voltage supply source. However, it does not disclose the resistor connected between a gate and a source of the transistor. Lee discloses the resistor (R703 in Fig. 4) connected between the gate and the source of the MOSFET (110 in Fig. 4). Both references have the same problem solving area, namely providing overcurrent and overvoltage electrical protection for the circuits. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Izawa solution by adding the resistor according to Lee, because as Lee states (col. 8, line 62 – col. 9, line 7), it is essential for fast turn-off of the MOSFET switch, which in turn, is essential element in the overvoltage protection activity.

Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Izawa et al. in view of Lee and Sellers (US 5,737,169). As per Claim 7, it differs from Claim 1 by its limitation of a resistor connected between the gate and the drain of the FET. Sellers discloses the resistor (32 in Fig. 1) connected between the gate and the drain of the FET (12 in Fig. 2). Both references have the same problem solving area, namely providing overcurrent and overvoltage protection for the circuits. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was

made to have further modified the Izawa solution by adding the resistor according to Sellers, because as Sellers states (col. 4, lines 42 – 62), the resistor helps to detect an overvoltage and to take appropriate measure.

Regarding Claim 8, Lee discloses the resistor interposed on the second connection line (R703 in Fig. 4). A motivation for modification of the primary reference is the same as above.

Claims 9 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Izawa et al. in view of Lee and Galecki (US 6,362,943). As per Claim 9, it differs from Claim 1 by its limitation of IGBT element, which is not disclosed by Izawa. Galecki discloses the circuit protecting the equipment against over-voltages and using the IGBT (IGBT in Fig. 5) as a control element. In the circuit of Fig. 5 no zener diodes are used as protection elements; the diode D1 plays only a role of the voltage stabilizer, thus satisfying the negative limitation conditions. Both references have the same problem solving area, namely providing protection to the equipment, including an overcurrent and overvoltage protection. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Izawa solution by replacing the NOSFET element by IGBT, because as Galecki states (col. 4, lines 15 – 27), the IGBT has substantial advantages against MOSFET, such as high breakdown voltage, up to 1000V.

As per Claim 11, it differs from Claim 9 by its limitation of the IGBT gate being connected to a gate drive supply source. Izawa et al. disclose the connection line connecting the IGBT gate to a gate drive supply source (elements 15 and 16 in Fig. 2).

Allowable Subject Matter

1. Claims 4 – 6 are allowed. A reason for that is that Claim 4 recites, *inter alia*, a limitation of a first resistor interposed on a second connection line between the gate and the source of the FET. Such limitation was not found in the collected prior art of the record.
2. Claims 2 and 3 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. A reason for that is that Claim 2 recites, *inter alia*, a limitation of a second resistor interposed between the gate and the first connection changer or between the first connection changer and the ground. Such limitation was not found in the collected prior art of the record.
3. Claims 10 and 12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. A reason for that is that the Claim 10 recite, *inter alia*, a limitation of a second resistor interposed between the gate of the IGBT and the connection changer or between the connection changer and the ground, while Claim 12, recites, *inter alia*, a limitation of a second resistor interposed on route from the gate of the IGBT to the ground through the connection line and the

connection changer. Such limitation was not found in the collected prior art of the record.

Response to Arguments

Applicant's Arguments have been given careful consideration but they are moot in view of the new ground of rejection. However, one argument is to be addressed. Applicant alleges that entry of the current amendment does not raise any new issue requiring further search and /or consideration (page 6, 3rd paragraph). However, the Amendment does present the new issue, since the Examiner did not considered the Claims 1, 4, 9 and 11 as having additional limitations introduced by the Amendment. As evident from current Office Action, the search revealed the new prior art, which is always helps to better define the scope of the invention.

Conclusion

1. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zeev Kitov whose current telephone number is (571) 272 - 2052. The examiner can normally be reached on 8:00 – 4:30. If attempts to reach examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (571) 272 – 2800, Ext. 36. The fax phone number for organization where this application or proceedings is assigned is (571) 273-8300 for all communications.

Z.K.
08/05/2005



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